REMARKS AND ARGUMENTS

Status Of The Claims

The present application includes pending claims 1-15. Claims 1-15 are rejected under 35 USC § 103(a).

Claims 1, 8-9, 12, 14-15 are rejected under 35 USC § 103(a) as being unpatentable over Puar et al (US 6,356,497) in view of McCormack et al (United States Patent No. 6,395,591).

Claims 11 and 13 are rejected under 35 USC § 103(a) as being unpatentable over McCormack et al and Puar et al, as applied to claim 1 above, and further in view of Wei (United States Patent No. 6,403,992).

Claims 1-15 are rejected on the grounds of non-statutory obviousness-type double patenting as being unpatentable over claim 1-6, 9-12 of United States Patent No. 6,995,431.

Claim 1, 2, 6 and 14 are currently amended.

Claims 3-5, 7-13, and 15 are as previously presented or original.

The Applicant respectfully submits that the claims define patentable subject matter. Accordingly, the Applicant respectfully traverses these rejections and requests reconsideration of the claims in view of the following remarks.

Patent Examination

Initially, the Applicant notes that a goal of patent examination is to provide a prompt and complete examination of a patent application.

> It is essential that patent applicants obtain a prompt yet complete examination of their applications. Under the principles of compact prosecution, each claim should be reviewed for compliance with every statutory requirement for patentability in the *initial review* of the application, even if one or more claims are found to be deficient with respect to some statutory requirement. Thus, Office personnel *should* state *all* reasons and bases for rejecting claims in the *first* Office action. Deficiencies should be explained clearly, particularly when they serve as a basis for a rejection. Whenever practicable, Office personnel should indicate how rejections may be overcome and how problems may be resolved. A failure to follow this approach can lead to unnecessary delays in the prosecution of the application.

Manual of Patent Examining Procedure (MPEP) § 2106(II). As such, the Applicant assumes, based on the goals of patent examination noted above, that the present Office Action has set forth "all reasons and bases" for rejecting the claims.

Claim Rejections Under 35 U.S.C. § 103

With regard to an obviousness rejection, in order for a *prima facie* case of obviousness to be established, the MPEP § 2142 states that the following three basic criteria must be met:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants disclosure.

Manual of Patent Examining Procedure MPEP at § 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (*emphasis added*). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness.

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See Manual of Patent Examining Procedure MPEP at § 2142.

Further, MPEP § 2143.01 states that "**the mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination**," and that "**although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be *a suggestion or motivation in the reference* to do so'**" (citing In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)). Moreover, MPEP § 2143.01 also states that "**the level of ordinary skill in the art cannot be relied upon**

to provide the suggestion ...," citing *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ 2d 1161 (Fed. Cir. 1999).

Motivation to Combine References

The Applicants note that every claim rejection is based on obviousness. "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is **not** whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." MPEP at § 2141.02.

The law is well settled that "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so." *ACS Hospital Systems, Inc. v. Montfiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929 (Fed. Cir. 1984). It is not permissible to pick and choose among the individual elements of assorted prior art references to re-create the claimed invention, but rather "some teaching or suggestion in the references to support their use in the particular claimed combination" is needed. *Symbol Technologies, Inc. v. Opticon, Inc.* 935 F.2d 1569, 1576, 19 USPQ2d 1241 (Fed. Cir. 1991).

In *Ex parte Hiyamazi*, the Board of Patent Appeals and Interferences reversed a rejection based on a combination of references, stating, in part:

> Under 35 USC § 103, where the Examiner has relied upon the teachings of several references, the test is whether or not the reference viewed individually and collectively would have suggested the claimed invention to the person possessing ordinary skill in the art. Note *In re Kaslow*, 707 F.2d 1366, 107 USPQ 1089 (Fed.Cir. 1983). **It is to be noted, however, that citing references which merely indicate the isolated elements and/or features recited in the claims are known is not a sufficient basis for concluding that the combination of claimed references would have been obvious.** That is to say, there should be something in the prior art or a convincing line of reasoning in the answer suggesting the desirability of combining the claimed invention. Note *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed.Cir. 1986).

Ex parte Hiyamazi, 10 USPQ2d 1393, 1394 (Bd. Pat. App. & Interf. 1988) (Emphasis added).

The Applicants respectfully submits that the Office Action does not identify a proper motivation to combine the various references to reject the claims of the present application. Merely identifying isolated elements in the prior art is not enough to establish a *prima facie* case of obviousness, as shown below:

> [M]ere identification in the prior art of each element is insufficient to defeat the patentability of the combined subject matter as a whole. [*In re Rouffet*, 149 F. 3d 1350] at 1355, 1357 [(Fed. Cir. 1998)]. Rather, to establish a prima facie case of obviousness based on a combination of elements disclosed in the prior art, the Board must articulate the basis on which it concludes that it would have been obvious to make the claimed invention. *Id.* In practice, this **requires** that the Board "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." *Id.* at 1357-59. This entails consideration of both the "scope and content of the prior art" and "level of ordinary skill in the pertinent art" aspects of the Graham test.
>
> **When the Board does not explain the motivation, or the suggestion or teaching, that would have led the skilled artisan at the time of the invention to the claimed combination as a whole, we infer that the Board used hindsight to conclude that the invention was obvious. *Id.* at 1358.**

See in re Kahn, 441 F.3d 977 (Fed. Cir. March 22, 2006) (emphasis added).

As the MPEP dictates, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must **both be found in the prior art, and not based on applicant's disclosure."** *See* Manual of Patent Examining Procedure (MPEP) at § 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added). *The Applicants respectfully submit, however, that the Office Action merely cites portions of the various references that may, but do not necessarily, disclose isolated claim limitations.* The Office Action's statements regarding motivation to combine the references amount to no more than conclusory

statements of convenient assumptions about one of ordinary skill in the art, which is a factual question that cannot be resolved on "subjective belief and unknown authority." *See In re Lee*, 277 F.3d 1338, 1344 (Fed. Cir. 2002). The Office Action does not explain the motivation, suggestion, or teaching to combine the various references. Again, mere identification of isolated elements is not enough to establish a *prima facie* case of obviousness. **"[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements**." *See in re Kahn,* 441 F.3d 977 (emphasis added).

The Federal Circuit "case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). The "examiner can satisfy the burden of showing obviousness of the combination 'only by showing some **objective** teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teaching reference.'" *See in re Lee , 277 F. 3d at 1343, citing In re Fitch,* 972 F. 2d 1260, 1265 (Fed. Cir. 1992) (emphasis added).

Merely citing portions of separate and distinct references that may or may not disclose an isolated claim element, however, is not a proper identification of a motivation to combine. The law requires that the Office Action show an **objective** teaching to support the assertions regarding motivation to combine the references. Subjective opinion of "common knowledge" or "common sense" regarding a motivation to combine is not enough to establish a *prima facie* case of obviousness. The Applicants respectfully submit that the motivation to combine the references identified in the Office Action is based on subjective knowledge and convenient assumptions gleaned from Applicants' disclosure, instead of the prior art (as is required by the Federal Circuit). Thus, at least for these reasons, the Applicants respectfully submit that the claims should be in condition for allowance.

Claims 1, 8-9, 12, 14-15

The office action states, "Claims 1, 8-9, 12, 14-15 are rejected under 35 USC § 103(a) as being unpatentable over Puar et al (United States Patent No. 6,356,497) in view of McCormack et al (United States Patent No. 6,395,591)."

The Applicant respectfully submits that McCormack is different from Applicant's amended independent claim 1. McCormack at least fails to disclose a "shielding layer" as set forth in Applicant's claim 1.

Regarding claims 1, and 8-9, the Office Action states,

> "Puar (Fig. 5) discloses a system for reducing noise in a chip, the system comprising: a substrate layer (P substrate) integrated within the chip; a transistor well layer (N-Well) integrated within the chip; at least one transistor of a first transistor type (P-type) formed within the well layer; and a positive potential of a quiet voltage source Vdd (column 4, lines 59-63) that is coupled to the at least one transistor of the first transistor type.
>
> Puar does not disclose that the transistor well layer (N-Well) is shielded by a shielding layer.
>
> However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate 50. The transistor well layer is shielded by a p type-shielding layer 12, which has higher doping than the (p-) substrate 50. Accordingly, it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate and the transistor layer because as taught by McCormack, the forming of a shielding layer having a higher doping than the substrate would lower the resistance of substrate for improving latchup immunity (column 1, lines 19-24) and for providing immunity against parasitic substrate effects" (column 2, lines 55-59).

McCormack discloses,

> "...an integrated circuit fabrication process us[ing] a selective substrate implant process to provide a substrate structure which can provide decoupling of power supply noise, such

> as ground noise, between noisy and noise sensitive circuits and also immunity against latchup and electrostatic discharge." (Column 2, Lines 46-50) (Emphasis added).
>
> "The selective substrate implant process is used to formed [sic] a heavily doped p++ region 14." (Column 2, Lines 64-66) (Emphasis added).
>
> "[T]he heavily doped p++ region 14 are [sic] selectively placed in p-type substrate 10 to achieve either the purpose of enhancing latchup suppression or decoupling power supply noise or both." (Column 3, Lines 17-20).

The selective substrate implant process disclosed in McCormack,

> "...can be used to form heavily doped regions underneath P-wells in which input/output circuits are built." (Column 6, Lines 16-17) (Emphasis added).
>
> "Thus, the p++ regions serve the purpose of improving the latchup suppression ability of the input, output or I/O circuits." (Column 6, Lines 24-26) (Emphasis added).

McCormack further states that

> "...the actual heavily doped regions are not formed as a contagious [sic] layer underneath the shaded areas as is depicted in FIGS. 4 and 5. Rather, one having ordinary skilled in the art would understand that the heavily doped regions are formed only in areas where P-wells are to be built." (Column 6, Lines 40-44) (Emphasis added).

McCormack suggests that the doping for both the P-type substrate 10 and the p-type epi layer 12 are in the same 14-28 ohm-cm range. (Compare Column 5, Line 47 with Column 6, Lines 2-3)

Even if the heavily doped p++ region 14 in McCormack functions as a "shielding" region, which the Applicant asserts it does not, the heavily doped p++ region 14 in McCormack cannot function as a shielding layer since it only covers a portion of the substrate layer. In fact, not only does McCormack fail to disclose a "shielding layer," McCormack actually teaches away from a "shielding layer." In Column 6, Lines 40-44, McCormack states that "one having ordinary skilled in the art would understand that the

heavily doped regions are formed only in areas where P-wells are to be built." (Emphasis added).

The Applicant respectfully asserts that, since epitaxial substrates have a low bulk resistivity material underneath the epitaxial layer, the epitaxial layers will couple noise more efficiently to nearby circuits or layers. Accordingly, since the epitaxial substrate or layer will couple the noise more efficiently to neighboring layers, it does not act as a shielding layer. Rather, the opposite is true and the epitaxial layer will act as a conductor of noise.

Claims 1, and 8-9

Regarding the rejection to claims 1, and 8-9, the Office Action concedes, "Puar does not disclose that the transistor well layer (N-Well) is shielded by a shielding layer." Accordingly, the Office Action looks to McCormack to satisfy this deficiency. In particular, the Office Action alleges the McCormack's "transistor well layer is shielded by a p type-shielding layer 12, which has a higher doping than the (p-) substrate 50." The Office Action then makes the erroneous assumption that "it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate and the transistor layer, because as taught by McCormack, the forming of a shielding layer having a higher doping than the substrate would lower the resistance of substrate for improving latchup immunity (column 1, lines 19-24), and for providing immunity against parasitic substrate effects (column 2, lines 55-59).

In response to the rejection to claims 1, and 8-9, the Applicant respectfully asserts that it is a well-founded scientifically proven fact that p-type epitaxial layer substrates have a low bulk resistivity material underneath the epitaxial layer, and as a result, the epitaxial layers will couple noise more efficiently to nearby circuits or layers. See the following hypertext link for support:

http://www.mosis.org/Faqs/tech_analog_ic_epi_substrate.pdf

Accordingly, since the epitaxial substrate or layer, such as the "p-type shielding layer 12" of McCormack will couple the noise more efficiently to

neighboring layers, it does not , and will not, act as a shielding layer. Rather, the epitaxial layer, such as the "p-type shielding layer 12" of McCormack, will act as a conductor of noise, and will cause noise to be coupled to neighboring layers regardless of whether the p type-shielding layer 12 has a higher doping than the (p-) substrate 50. (Emphasis added).

Claim 8 depends from claim 1, and claim 9 also depends from claim 1, the latter of which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicants respectfully asserts that amended claims 1, and 8-9 define patentable subject matter, and are therefore in condition for allowance. The Applicants respectfully request allowance of claims 1, and 8-9.

Claims 14-15

With regard to the rejection to claims 14 and 15, the Office Action states,

> "Regarding claims 14-15, Puar (Fig. 5) further discloses a noisy voltage source 38 of positive (column 4, lines 59-63) coupled to a source of the transistor."

In response, the Applicant respectfully asserts that claim 14 depends from claim 1, the latter of which is believed to be allowable. Claim 15 depends from claim 14, the latter of which depends from a base claim, namely claim 1, which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that claims 14 and 15 define patentable subject matter, and are therefore in condition for allowance. The Applicant respectfully requests allowance of claims 14 and 15.

Claim 12

Regarding the rejection to claim 12, the Office Action states,

> "McCormack (Fig. 2) further teaches that the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 16/18/22."

In response, the Applicant respectfully asserts that claim 12 depends from claim 1, the latter of which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that claim 12 defines patentable subject matter, and is therefore in condition for allowance. The Applicant respectfully requests allowance of claim 12.

Claims 1-10, 12, and 14-15

The Office Action states,

> "Regarding claims 1-10, 12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (US. 6,395,591) in view of Puar et a1 (US. 6,356,497).
>
> Regarding claims 1, 8-9 and 12, McCormack (Fig. 2) discloses a system in a chip, the system comprising: a substrate layer 10 integrated within the chip; a transistor well layer 16/18/22 within the chip, which is shielded from the substrate layer 10 by a shielding layer 12; a transistor 30 of a first transistor type (P type) disposed within the transistor well layer 22, wherein the transistor well layer 22 is coupled to the shielding layer 12, and the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 22.
>
> McCormack does not disclose a positive potential of a quiet voltage source coupled to the transistor 30.
>
> However, Puar (Fig. 5) teaches the forming of a system for reducing noise in a chip, the system comprising a transistor of P type disposed in a transistor well layer (N-Well) and having a positive potential Vdd of a quiet voltage source (column 4, lines 59-63) coupled to the transistor. Accordingly, it would have been obvious to couple a positive potential of a quiet voltage source to the transistor well layer

> (N-Well) of the transistor 30 of McCormack because such coupling of positive quiet voltage source to the transistor well layer would prevent the noise generated from the noisy substrate voltage, as taught by Puar" (column 4, lines 55-65).

In response to the rejection to claims 1, and 8-9, the Applicant respectfully asserts that it is a well-founded scientifically proven fact that p-type epitaxial layer substrates have a low bulk resistivity material underneath the epitaxial layer, and as a result, the epitaxial layers will couple noise more efficiently to nearby circuits or layers. See the following hypertext link for support:

http://www.mosis.org/Faqs/tech_analog_ic_epi_substrate.pdf

Accordingly, since the epitaxial substrate or layer, such as the "p-type shielding layer 12" of McCormack will couple the noise more efficiently to neighboring layers, it does not , and will not, act as a shielding layer. Rather, the epitaxial layer, such as the "p-type shielding layer 12" of McCormack, will act as a conductor of noise, and will cause noise to be coupled to neighboring layers regardless of whether the p type-shielding layer 12 has a higher doping than the (p-) substrate 50. (Emphasis added).

Since the p-type epitaxial layer 12 does not and cannot function as a shielding layer, neither McCormack, nor Puar, nor McCormack in view of Puar disclose the limitation of "a transistor layer integrated within the chip, which is shielded from the substrate layer by a shielding layer, wherein said shielding layer reduces noise in the chip" as stated in the Applicant's claim 1. Claim 1 should therefore be allowable. Furthermore, claim 8 depends from claim 1, and claim 9 also depends from claim 1, the latter of which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that amended claims 1, and 8-9 define patentable subject matter, and are therefore in condition for allowance. The Applicant respectfully requests allowance of claims 1, and 8-9.

Claims 2-7

The Office Action states,

> "Regarding claims 2-7, McCormack (fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28."

In response, the Applicant respectfully asserts that claim 2 depends from claim 1, the latter of which is believed to be allowable. Claims 2-6 depend from claim 2, the latter of which depends from a base claim, namely claim 1, which is believed to be allowable. Claim 7 depends from claim 6, the latter of which depends from claim 2, the latter of which depends from a base claim, namely claim 1, which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that claims 2-7 define patentable subject matter, and are therefore in condition for allowance. The Applicant respectfully requests allowance of claims 2-7.

Claim 10

The Office Action states,

> "Regarding claim 10, McCormack (Fig. 2) further discloses that the transistor 30 has a transistor well layer 22 of N type is capacitively coupled to the shielding layer 12 of P type."

In response, the Applicant respectfully asserts that claim 10 depends from claim 1, the latter of which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that claim 10 define patentable subject matter, and is therefore in condition for allowance. The Applicant respectfully requests allowance of claim 10.

Claims 14-15

The Office Action states,

> "Regarding claims 14-15, Puar (Fig. 5) also teaches a noisy voltage 38 (column 4, lines 59-63) coupled to the transistor source of a first transistor type (P type)."

In response, the Applicant respectfully asserts that claim 14 depends from claim 1, the latter of which is believed to be allowable. Claim 14 depends from claim 14, the latter of which depends from a base claim, namely claim 1, which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that claims 14 and 15 define patentable subject matter, and are therefore in condition for allowance. The Applicant respectfully requests allowance of claims 14 and 15.

Claims 11 and 13

The Office Action states,

> "Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al and Puar et al as applied to claim 1 above, and further in view of Wei (US. 6,403,992).
>
> McCormack discloses the shielding layer 12 is deep P-well, but not N-well which is capacitively coupled to the substrate layer 10. However, Wei teaches the convention of forming a transistor within a shielding layer of P-well, which is capacitively coupled to the N type substrate (Fig. 3), or a transistor within a shielding layer of N-well, which is capacitively coupled to the P type substrate (Fig. 4).
>
> Accordingly, it would have been obvious to form the shielding layer 12 of McCormack with either N type or P type because they both provide the benefits of eliminating substrate effect, as taught by Wei (column 1, lines 47-60)."

In response to the rejection to claims 11 and 13, the Applicant respectfully asserts that it is a well-founded scientifically proven fact that p-type epitaxial layer substrates have a low bulk resistivity material underneath the epitaxial layer, and as a result, the epitaxial layers will couple noise more efficiently to nearby circuits or layers. See the following hypertext link for support:

http://www.mosis.org/Faqs/tech_analog_ic_epi_substrate.pdf

Accordingly, since the epitaxial substrate or layer, such as the "p-type shielding layer 12" of McCormack will couple the noise more efficiently to neighboring layers, it does not , and will not, act as a shielding layer. Rather, the epitaxial layer, such as the "p-type shielding layer 12" of McCormack, will act as a conductor of noise, and will cause noise to be coupled to neighboring layers regardless of whether the p type-shielding layer 12 has a higher doping than the (p-) substrate 50. (Emphasis added).

Since the p-type epitaxial layer 12 does not and cannot function as a shielding layer, neither McCormack, nor Puar, nor McCormack in view of Puar disclose the limitation of "a transistor layer integrated within the chip, which is shielded from the substrate layer by a shielding layer, wherein said shielding layer reduces noise in the chip" as stated in the Applicant's claim 1. Claim 1 should therefore be allowable. Furthermore, claim 11 depends from claim 1, and claim 13 also depends from claim 1, the latter of which is believed to be allowable.

The Applicant further respectfully asserts that the N-well 484 of Wei is **not a shielding layer**, which eliminates the substrate effect, **which reduces noises transfer**. (Emphasis added). As stated in Wei, with reference to FIG. 1, "the N-type substrate of the high voltage PMOS 10 and N-type substrate of the low voltage PMOS 12 communicate with each other via the underlying N-type substrate." As a result, "the voltage level of the substrate (B4) of the low PMOS 12 is equal to that of the substrate (B2) of the high voltage PMOS 10." This causes a "**serious body effect** [to] occur[] to the low voltage PMOS 12." Accordingly, "as the substrate voltage level of the low voltage PMOS 12 increases, the reverse bias from the source (S4) of the low voltage PMOS 12 to the substrate (B4) is increased to cause an increase of the threshold

voltage of the low voltage PMOS 12. When the input operation voltage is a low voltage, the low voltage PMOS 12 cannot operate normally."

A similar body effect occurs with P-type substrates. Wei, with reference to FIG. 2 states, "Since the P-wells of the high voltage NMOS 24 and the low voltage NMOS 26 conduct via the underlying P-type substrate, the substrate (B3 and B1) voltage levels of the low voltage NMOS 26 and the high voltage NMOS 24 are the same." As a result, "A serious body effect is caused." Wei further states, "As the substrate (B3) voltage level of the low voltage NMOS 26 decreases, the reverse bias from the source (S3) of the low voltage NMOS 26 to the substrate (B3) increases to cause an increase in threshold voltage of the low voltage NMOS 26." Accordingly, similar to the case of the N-type substrate, "When the input voltage is a high voltage, the low voltage NMOS 26 cannot function properly."

Wei discloses in FIG. 2 and FIG. 3, a conventional method for a "CMOS device to obtain multiple voltage levels with the elimination of substrate effect," which is described above with respect to FIG. 1 and FIG. 2. As stated in Wei, with reference to FIG. 3, for "a CMOS device with an N-type substrate [] ... An additional P-well 382 is added in the low voltage CMOS area of the CMOS device, so that the problem caused by conductance between the N-wells is resolved." "**The body effect is thus eliminated** and the low voltage PMOS 32 can function normally." **In other words, the addition of the additional P-Well 382 eliminates the "body effect," which occurs as a result of the conductance in the N-wells.**

A similar situation occurs with CMOS devices with a P-type substrate. As stated in Wei, with reference to FIG. 4, for "a CMOS device with a P-type substrate [] ... An additional N-well 484 is added in the low voltage CMOS area of the CMOS device so that the problem caused by communication between the P-wells is resolved." **The body effect is thus eliminated**, and the low voltage NMOS 46 can operate normally. **In other words, the addition of the additional N-Well 484 eliminates the "body effect," which occurs as a result of the conductance in the P-wells.**

Accordingly, the Applicant respectfully asserts that the addition of the additional

P-Well 382 eliminates the "body effect," which occurs as a result of the conductance in the N-wells. **The additional P-Well 382 does not act as a shielding layer to reduce noise transfer in the device.** Similarly, the addition of the additional N-Well 484 eliminates the "body effect," which occurs as a result of the conductance in the P-wells. **The additional N-Well 484 does not act as a shielding layer to reduce noise transfer in the device.**

Furthermore, **the Applicant respectfully asserts that, since epitaxial substrates, whether P-type or N-type, have a low bulk resistivity material underneath the epitaxial layer, the epitaxial layers will couple noise more efficiently to nearby circuits or layers. Accordingly, since the epitaxial substrate or layer will couple the noise more efficiently to neighboring layers, it does not act as a shielding layer. Rather, the opposite is true and the epitaxial layer will act as a conductor of noise.**

Accordingly, at least for the reasons cited herein, the Applicant respectfully assert that amended claims 11 and 13 define patentable subject matter, and are therefore in condition for allowance. The Applicant respectfully requests allowance of claims 11 and 13.

In response to the rejection to claims 1, and 8-9, the Applicant respectfully asserts that it is a well-founded scientifically proven fact that p-type epitaxial layer substrates have a low bulk resistivity material underneath the epitaxial layer, and as a result, the epitaxial layers will couple noise more efficiently to nearby circuits or layers. See the following hypertext link for support:

http://www.mosis.org/Faqs/tech_analog_ic_epi_substrate.pdf

Accordingly, since the epitaxial substrate or layer, such as the "p-type shielding layer 12" of McCormack will couple the noise more efficiently to neighboring layers, it does not , and will not, act as a shielding layer. Rather, the epitaxial layer, such as the "p-type shielding layer 12" of McCormack, will act as a conductor of noise, and will cause noise to be coupled to neighboring layers regardless of whether the p type-shielding layer 12 has a higher doping than the (p-) substrate 50. (Emphasis added).

Since the p-type epitaxial layer 12 does not and cannot function as a shielding layer, neither McCormack, nor Puar, nor McCormack in view of Puar disclose the limitation of "a transistor layer integrated within the chip, which is shielded from the substrate layer by a shielding layer, wherein said shielding layer reduces noise in the chip" as stated in the Applicant's claim 1. Claim 1 should therefore be allowable. Furthermore, claim 8 depends from claim 1, and claim 9 also depends from claim 1, the latter of which is believed to be allowable.

Accordingly, at least for the reasons cited herein, the Applicant respectfully asserts that amended claims 1, and 8-9 define patentable subject matter, and are therefore in condition for allowance. The Applicant respectfully requests allowance of claims 1, and 8-9.

Double Patenting Rejection

Claims 1-15 are rejected on the grounds of non-statutory obviousness-type double patenting as being unpatentable over claim 1-6, 9-12 of United States Patent No. 6,995,431.

The Applicant is filing herewith, a Terminal Disclaimer in Compliance with 37 C.F.R § 1.321(c), so as to overcome this non-statutory obviousness-type double patenting rejection.

Response to Examiner's Arguments

Examiner's Response to Arguments

Paragraph 8, page 7 of the Office Action states:

> "Applicant argues that it would not be obvious to combine McCormack with Puar because McCormack fails to disclose "a shielding layer". According to Applicant, the P type epitaxy layer 12 does not function as "a shielding layer" for reducing noise in a chip.
>
> This argument is not persuasive because of the following reasons:
>
> First, the limitation of having "a shielding layer" functioning as reducing noise in a chip does not seem to be required by the claim language because it is not stated in the claims. It is the claims that define the claimed invention, and it is claims, not specifications that are anticipated or unpatentable. *Constant* v. *Advanced Micro-Devices Inc.,* '7 USPQ2d 1064. Therefore, the P type epitaxy layer would function as "a shielding layer" because this layer is disposed between the substrate layer 1 0 and the transistor well layers for isolating or shielding the transistor well layers from the substrate layer 10.
>
> Second, in contrary to Applicant's assertions, McCormack clearly states at column 4, lines 25-29 that "Digital switches and power MOSFET *generated substrate noise* during switching operations. In particular, power MOSFETs, typically used to provide one to three amperes of output current, can generate a substantial amount of shoot-through current." Therefore, the P type epitaxy layer 12 would inherently function as "a shielding layer" for reducing the noise transfer to the substrate layer 10 from the noise generated during switching operation of the switches and power MOSFETs formed in the transistor well layers because the epitaxy layer 12 is disposed between the substrate layer 10 and the transistor well layers to isolate the substrate layer 10 from the transistor well layers.

> Applicant is noted that since the examiner presents evidence or reasoning tending to show inherency, the burden shifts to Applicant to show an unobvious different. Therefore, if Applicant belies that the P type epitaxy layer 12 would not function as an isolating layer or "shielding layer" even though it is disposed between the substrate layer 10 and the transistor well layers, then Applicant is requested to support that position with facts.

Applicant's Response to Arguments

In response to the argument that "the limitation of having "a shielding layer" functioning as reducing noise in a chip does not seem to be required by the claim language because it is not stated in the claims," the Applicant has amended Claim 1 to recite, inter alia, "**a transistor layer integrated within the chip, which is shielded from said substrate layer by a shielding layer, wherein said shielding layer reduces noise in the chip.**" (New material underline.) Accordingly, the Examiner argument is now moot.

In response to the argument that the "P type epitaxy layer 12 would inherently function as "a shielding layer" for reducing the noise transfer to the substrate layer 10 from the noise generated during switching operation of the switches and power MOSFETs formed in the transistor well layers because the epitaxy layer 12 is disposed between the substrate layer 10 and the transistor well layers to isolate the substrate layer 10 from the transistor well layers," the Applicant respectfully asserts that such as statement is erroneous, without merit, and contrary to technical findings, at least for the following reasons. The Applicant expressly reserves the right to present additional reasons why the statement is erroneous, without merit, and/or contrary to technical findings.

In general, the use of an epitaxial substrate is generally preferred because these types of wafers permit IC designs that are significantly more robust against latch-up than other designs that utilize bulk silicon wafers. Most submicrometer fabrication lines use epitaxial wafer starting material for digital IC fabrication because of the improved latch-up robustness. Although analog designs may benefit from latch-up robustness,

other factors favor using bulk wafer starting material.

Analog designs require good isolation between circuits to achieve low noise performance. A bulk substrate, with its high bulk resistivity, acts as a filter to attenuate high frequency noise rapidly minimizing coupling to surrounding circuitry. **Since epitaxial substrates have a low bulk resistivity material underneath the epitaxial layer, epitaxial layers are able to couple noise more efficiently to nearby circuits or layers. Accordingly, since the epitaxial substrate or layer will couple the noise to neighboring layers, it does not act as a shielding layer.** Also, the presence of a low resistivity layer under the epitaxial layer will cause spiral inductors to have lower Q due to the close proximity of the lower resistivity bulk substrate. Support for this may be found in the document at "http://www.mosis.org/Faqs/tech_analog_ic_epi_substrate.pdf" (herein after "The Epi-Substrate document"), which is hereby incorporated herein in its entirety. The Epi-Substrate document also cites numerous references in support.

The Epi-Substrate document states,

> **Question:**
> What is the advantage/disadvantage of using epitaxial substrates in analog or mixed signal IC designs?
>
> **Answer:**
> There are a number of factors to consider when choosing epitaxial wafers for IC designs. Epitaxial substrate starting material is preferred because these wafers permit IC designs that are significantly more robust against latch-up than designs using bulk silicon wafers. Most submicrometer fabrication lines use epitaxial wafer starting material for digital IC fabrication because if the improved latch-up robustness. Although analog designs will benefit from latch-up robustness other factors favor using bulk wafer starting material. Analog designs require good isolation between circuits to achieve low noise performance. A bulk substrate, with its high bulk resistivity, acts as a filter to attenuate high frequency noise rapidly minimizing coupling to surrounding circuitry. Epitaxial substrates have a low bulk resistivity material underneath the epitaxial layer which is able to couple noise more efficiently to nearby circuits. Also, the presence of a low resistivity layer under the epitaxial layer will cause spiral inductors to have lower Q due to the close proximity of the lower resistivity bulk substrate. As a result of

these design issues, most foundries that advertise mixed signal IC fabrication will offer either epitaxial wafers or bulk wafers as options to please both digital designers and analog designers.

Substrate Coupling References:

P. Basedau & H. Qiuting, ``A post processing method for reducing substrate coupling in mixed-signal integrated circuits," Symposium on VLSI Circuits, Kyoto, 8-10 June, pp. 41-42, 1995.

K.J Kerns, I.L. Wemble & A.T. Yang, ``Efficient parasitic substrate modeling for monolithic mixed-A/D circuit design and verification," Analog Integrated Circuits and Signal Processing, Vol. 10, No. 1-2, pp. 7-21, June-July 1996.

K. Makie-Fukuda, S. Maeda, T. Tsukada & T. Matsuura, ``Substrate noise reduction using active guard band filters in mixed-signal integrated circuits," Symposium on VLSI Circuits, Kyoto, 8-10 June, pp. 33-34, 1995.

S. Masui, ``Simulation of substrate coupling in mixed-signal MOS circuits," Symposium on VLSI Circuits, Seattle, 4-6 June, pp. 42-43, 1992.

D.K. Su, M.J. Loinaz, S. Masui & B.A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," IEEE Journal of solid State Circuits, Vol. 28, No. 4, pp. 420-430, April 1993.

N.K. Verghese, D.J. Allstot & M.A. Wolfe, ``Verification techniques for substrate coupling and their application to mixed-signal IC design," IEEE Journal of Solid State Circuits, Vol. 31, No. 3, pp. 345-365, March 1996.

"Modeling and Analysis of Substrate Coupling in Integrated Circuits" by R. Gharpurey and R. G. Meyer in the proceedings of the Custom Integrated Circuits Conference, May 2-4, 1995, Santa Clara.

URL to a Masters Thesis - "Modeling of High Speed Metal-Insulator-Semiconductor Interconnections: The Effect of ILD on Slow-Wave Attenuation"

http://inp.cie.rpi.edu/research/mcdonald/frisc/theses/LWangThesis/LWangThesis.html

URL to an on-line paper: "Analysis and Simulation of Substrate Coupling in Integrated Circuits" http://bwrc.eecs.berkeley.edu/Publications/1994/subtrate_coupling.ijcta/index.html

Some General IC Design References:
P. Gray and R. Meyer, Analysis and Design of Integrated Circuits, 3rd edition, Wiley, 1993.

Y. Tsividis, Mixed Analog-Digital VLSI Devices and Technology, McGraw-Hill, 1996.

T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.

Laker and Sansen, Design of Analog Integrated Circuits and Systems, McGraw-Hill, 1994."

Since the Office Action alleged that "the examiner present[ed] evidence or reasoning tending to show inherency," which the Applicant respectfully disagrees, "the burden shifts to Applicant to show an unobvious difference." In view of the Epi-Substrate document and its reference, the Applicant respectfully factually asserts that the "P type epitaxy layer 12 would not function as an isolating layer or "shielding layer" even though it is disposed between the substrate layer 10 and the transistor well layers." The Applicant further respectfully asserts that an unobvious difference has been shown and the Applicant has satisfied the required burden of proof.

At least for these reason, the Applicant respectfully request that the rejections to claim 1-15 be withdrawn. Accordingly the Applicant respectfully request that claims 1-15 be allowed.

CONCLUSION

Based on the foregoing, the Applicant believes that all claims 1-15 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Attorney at (312) 775-8191.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Terminal Disclaimer in Compliance with 37 C.F.R § 1.321(c), is being filed herewith, in order to overcome the non-statutory obviousness-type double patenting rejection.

A Notice of Allowability is courteously solicited.

Respectfully submitted,

Date: September 13, 2006

Ognyan I. Beremski, Esq.
Registration No. 51,458
Attorney for Applicant(s)

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(312) 775-8000

HSW